

## ABSTRACT OF THE DISCLOSURE

## PULSE-CONTROLLED MICROPIPELINE ARCHITECTURE

5 A control circuit for permitting a two-phase data  
transfer protocol between stages in a micropipeline. In  
accordance with the teachings of the present invention,  
the control circuit includes a control element for  
generating a data transfer control signal that governs  
10 data transport through a level-sensitive latch within the  
micropipeline. The control circuit further includes a  
dual-pulse generator receiving the data transfer control  
signal at its input and providing its output to the  
control input of the level-sensitive latch. The dual  
15 pulse generator converts a rising edge of the data  
transfer control signal into a first data transfer pulse  
and a falling edge of the data transfer control signal  
into a second data transfer pulse such that the  
micropipeline transfers data during both the rising edge  
20 and the falling edge.

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